



Southern Illinois University System

### Applications

- Live video broadcasting
  - Sporting events
  - 4K TV
  - AR and VR
- Fast responsive video-based systems
  - Self-driving vehicles
  - Drone operation
  - Security systems
  - Surveillance systems

### Inventor(s)

Chao Lu, (PhD, Purdue University)

*Dr. Lu is an assistant professor of electrical and computer engineering at SIU Carbondale. His research focuses on system-level optimization, and HEVC/H.265 video/image processing architecture.*

Yuanzhi Zhang

*Mr. Zhang is a Ph.D. student researcher of department of electrical and computer engineering at SIU Carbondale. His research interests include VLSI architecture design of multi-media SoC, HEVC algorithm optimization*

### Contact

Daniel Ashbaugh, JD  
Technology Transfer  
Specialist  
[dashbaugh@siu.edu](mailto:dashbaugh@siu.edu)  
(618) 453-4544

## Highly Parallel Hardware Architecture for H.265/HEVC Bit Rate Estimator

HEVC (H.265) debuted in 2013 as a new UHD video compression standard. Though H.265 offers superior performance to legacy H.264 technologies, a dramatic increase in computational complexity has led to processing delays for software-based HEVC intra encoders that make them unsuitable for real-time video encoding applications. Bit rate estimation is typically the most time-consuming step in video encoding. A primary challenge has thus been to develop reliable, efficient hardware architectures for bit rate estimation to enable real-time high-quality UHD video encoding (e.g. 4K@30fps).

### Invention

SIU researchers have developed a highly parallel hardware bit rate estimator in compliance with the HEVC standard. The bit rate estimator features five parallel syntax groups and a CABAC scheme that incorporates feedback to update the context model and improve accuracy. The design has been implemented in Verilog and synthesized in FPGA and ASIC.

### Key Advantages

- Supports 4x4 PU and 8x8 up to 64x64 CUs
- Improved estimation accuracy (BD\_Rate 0.0518%)
- Higher throughput
- Low hardware cost/area (15.5k gates) and power consumption (9.8 mW)

### Status

U.S. nonprovisional patent application #16/389,092 was filed April 19, 2019. The technology is available for license.

*Other opportunities related to this technology, included but not limited to sponsored and/or collaborative research, may be available. Please reach out to the designated contact identified at left for more information.*